REMARKS

Reconsideration of the above-identified patent application in view of the amendments above and the remarks following is respectfully requested.

Claims 1-23 and 26-28 are in this case. Claims 1, 7, 18, 23 and 26 have been rejected under § 102(b). Claims 1, 7, 18, 23 and 26 have been rejected under § 102(e). Claims 1-23 and 26-28 have been rejected under § 103(a). Dependent claims 4 and 9 have been canceled. Independent claims 1, 7, 18, 23 and 26 and dependent claims 2, 3, 5, 8, 10-17, 19, 21 and 27 have been amended. New independent claims 29-32 have been added.

The claims before the Examiner are directed toward methods of assembling and testing electronic devices, specifically, systems-in-package (SIPs), and to a device so assembled and tested. A CPU, a nonvolatile memory and a volatile memory are fabricated on respective, physically independent chips and are packaged together in a common package with the CPU operationally connected to the memories. Testing programs, for testing the memories by writing to the memories, are stored in the nonvolatile memory and are executed by the CPU from the volatile memory to test the memories. Then the CPU is tested. The results of the tests of the memories are stored in the nonvolatile memory.

§ 103(a) Rejections – Chesley '142 in view of AAPA

The Examiner has rejected claims 1-5, 7-16, 18-21, 23, 26 and 27 under § 103(a) as being "unpatented" (Applicant presumes the Examiner meant "unpatentable") over Chesley, US Patent No. 4,333,142 (henceforth, "Chesley '142") in view of Applicant Admitted Prior Art (henceforth, "AAPA"). The Examiner's rejection is respectfully traversed.

Chesley '142 teaches a computer fabricated on a single wafer **11** with redundant components and configured to test itself when power is applied to identify and not use inoperative components. Specifically, the computer includes many CPU chips **12**, many ROM chips **13** and many RAM chips **14**. When power is applied to the computer, each CPU tests itself until a working CPU is found. The working CPU does checksum testing of the ROMs until a working ROM is found. The working CPU then runs a test routine stored in the working ROM to test itself and also runs another test routine stored in the working ROM to test the RAMs in order to identify working RAMs.

The AAPA cited by the Examiner is fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP.

Applicant respectfully submits that the Examiner has failed to establish *prima facie* obviousness of some of the rejected claims.

According to MPEP 2143.03, in order for *prima facie* obviousness of a claim to be established, all the claim limitations must be taught or suggested by the cited references. This is not the case with regard to independent claims 18, 23 and 26 and dependent claims 4 and 12.

In the case of independent claim 18, the prior art cited by the Examiner fails to teach or suggest step (e), executing a testing program by the CPU in order to test the nonvolatile memory. The first working CPU of Chesley '142 tests itself and the RAMs by executing test routines stored in the first working ROM, but test the ROMs, not by executing test routines stored in the ROMs, but by adding the contents of the ROMs and comparing those contents to checksums stored in the ROMs. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips

and assembling and packaging the chips in a SIP and is silent about testing the memories.

In the case of independent claim 23, the prior art cited by the Examiner fails to teach or suggest that a program for testing the nonvolatile memory is stored in the nonvolatile memory. The ROMs of Chesley '142 store test routines for testing the CPUs and the RAMs but not for testing the ROMs themselves. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about what is stored in the memories.

In the case of independent claim 26, the prior art cited by the Examiner fails to teach or suggest step (e) (now step (f)): storing, in the nonvolatile memory, results of testing the volatile memory. The nonvolatile memories of Chesley '142 are ROMs, so that test results could not be stored in those memories. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about storing test results.

It follows that independent claims 18, 23 and 26 are allowable in their present form over the combined teachings of Chesley '142 and AAPA. It then follows that claims 19-21 and 27 that depend therefrom also are allowable over the combined teachings of Chesley '142 and AAPA.

Dependent claim 4 adds to independent claim 1 the step of storing the results of testing the memory or memories in one of the memories, by the CPU. As noted above in the context of independent claim 26, Chesley '142 and AAPA neither teach nor suggest this limitation. (The discussion of Chesley '142 in the context of independent claim 26 actually only shows that Chesley '142 does not store results of testing his RAMs in one of his ROMs. Chesley '142 does not store these results in

any of his RAMs, either. The only test results stored by Chesley '142 is a list of working RAM addresses, that is stored in address register **28** of the working CPU.) Therefore, independent claim 1 has been amended to include the limitations of claim 4. Correspondingly, claim 4 has been canceled and claim 5 has been amended to depend directly from claim 1. With independent claim 1 allowable in its present form over the combined teachings of Chesley '142 and AAPA, it follows that claims 2, 3 and 5 that depend therefrom also are allowable over the combined teachings of Chesley '142 and AAPA.

Dependent claim 9 adds to independent claim 7 the step of loading a testing program into the volatile memory, with the CPU then testing at least one of the memories by executing that testing program. The prior art cited by the Examiner fails to teach or suggest this limitation. Chesley '142 executes the RAM test routine of the working ROM in-place, not by loading this routine into one of the RAMs and executing the routine in the RAM. The cited AAPA is confined to fabricating a CPU and one or more memories on separate chips and assembling and packaging the chips in a SIP and is silent about how the memories are tested. Therefore, independent claim 7 has been amended to include the limitations of claim 9. Correspondingly, claim 9 has been canceled and claim 10 has been amended to depend directly from claim 7. With independent claim 7 allowable in its present form over the combined teachings of Chesley '142 and AAPA, it follows that claims 8 and 10-16 that depend therefrom also are allowable over the combined teachings of Chesley '142 and AAPA.

Dependent claim 12 adds to independent claim 7 the step of storing the results of testing the memory or memories in the nonvolatile memory, by the CPU. As noted above in the context of independent claim 26, Chesley '142 and AAPA neither teach

nor suggest this limitation. Therefore, new claim 29 has been added. New claim 29 is claim 12 of the response filed May 8, 2006, rewritten in independent form.

§ 103(a) Rejections – Chesley '142 in view of AAPA and further in view of Takizawa '663

The Examiner has rejected claims 6, 17, 22 and 28 under § 103(a) as being unpatentable over Chesley '142 in view of AAPA and further in view of Takizawa, US Patent No. 6,198,663. The Examiner's rejection is respectfully traversed.

It is demonstrated above that independent claims 1, 7, 18 and 26 are allowable in their present form. It follows that claims 6, 17, 22 and 28 that depend therefrom also are allowable.

§ 102(b) Rejections – Helbig, Sr. et al. '273

The Examiner has rejected claims 1, 7, 18, 23 and 26 under § 102(b) as being unpatentable over (Applicant presumes the Examiner meant "anticipated by") Helbig, Sr. et al., US Patent No. 6,311,273 (henceforth, "Helbig, Sr. et al. '273"). The Examiner's rejection is respectfully traversed.

Claim 1 now has been amended to include the limitations of claim 4. Claim 7 now has been amended to include the limitations of claim 9. Because claims 4 and 9 were not rejected over Helbig, Sr. et al. '273, these amendments render claims 1 and 7 allowable over Helbig, Sr. et al. '273.

Helbig, Sr. et al. '273 teach an electronic circuit, including a coprocessor and a multiprocessor logic controller, that, when interposed between the CPU of a computer system and the rest of the computer system, allows a trusted operator to verify that the security of the computer system has not been compromised. For example, upon power up or system reset, the CPU and the coprocessor run built-in self-test routines.

Then the coprocessor computes the digital signatures of code stored in nonvolatile memories of the system, such as the BIOS, DOS, the interrupt tables, and the autoexec.bat and config.sys files to verify that the security of this code has not been compromised.

There are at least two significant differences between the teachings of Helbig, Sr. et al. '273 and the present invention. First, Helbig, Sr. et al. '273 test only nonvolatile memories. The present invention tests both nonvolatile memories and volatile memories. Second, the tests performed by Helbig, Sr. et al. '273 are tests of the contents of the nonvolatile memories, not tests of the operation of the nonvolatile memories. Specifically, Helbig, Sr. et al. '273 perform digital signature comparisons that require only reading data stored in the nonvolatile memories under test, not both reading and writing. By contrast, the kind of memory tests performed by the present invention is the same kind of memory tests performed according to the prior art, as described on page 2 lines 10-11 of the specification:

> ...each bit of the memory chip must be tested by writing to the bit and then reading the bit. (emphasis added)

It follows that independent claims 23 and 26 are not anticipated by Helbig, Sr. et al. ''273. The last limitation recited in claim 23 is that a program for testing the volatile memory is stored in the nonvolatile memory. Similarly, step (d) (now step (e)) of claim 26 recites testing a volatile memory. Furthermore, independent claims 23 and 26 are not even obvious from Helbig, Sr. et al. '273. The only memories of concern to Helbig, Sr. et al. '273 are those whose contents could be subject to attack by intruders, *i.e.*, nonvolatile memories. There is neither a hint nor a suggestion in Helbig, Sr. et al. '273 of a need to "test" volatile memories.

Independent claim 18 has been rendered allowable over Helbig, Sr. et al. '273 by amending step (d) of claim 18 to recite storing, in the nonvolatile memory, a

program that tests the nonvolatile memory by writing to the nonvolatile memory. Support for this amendment is found in the specification in the above citation from page 2 lines 10-11. For stylistic consistency, the name of the program has been changed in claims 18 and 19 from "testing program" to just "program".

§ 102(e) Rejections – Malladi et al. '825

The Examiner has rejected claims 1, 7, 18, 23 and 26 under § 102(e) as being unpatentable over (Applicant presumes the Examiner meant "anticipated by") Malladi et al., US Patent No. 6,636,825 (henceforth, "Malladi et al. '825"). The Examiner's rejection is respectfully traversed.

Claim 1 now has been amended to include the limitations of claim 4. Claim 7 now has been amended to include the limitations of claim 9. Because claims 4 and 9 were not rejected over Malladi et al. '825, these amendments render claims 1 and 7 allowable over Malladi et al. '825.

Malladi et al. '825 teach a method of testing a SIP. According to the prior art of which Malladi et al. '825 is an improvement, a SIP is made by mounting a microprocessor **11** and memories **13** and **15** on a substrate **17**. Then electrical connectors **19** are used for testing microprocessor **11** and for testing memories **13** and **15** via microprocessor **11**. According to Malladi et al. '825, a SIP is made in two steps. In the first step, only a microprocessor **31** is mounted on a substrate **37** and then tested. If microprocessor **31** passes the test, then memories **33** and **35** are mounted on substrate **37** and then are tested. The tests of the SIP components, as performed both by the prior art of which Malladi et al. '825 is an improvement and by Malladi et al. '825 themselves, are performed as described in the prior art manner described in the specification on page 2 lines 1-5:

> A SIP is tested much as an individually packaged chip is tested: by being mounted on a testing board, with testing pins connected to the external connectors of the SIP. Appropriate voltages are supplied to selected external connectors, and the responses of the SIP at the same external connectors or at other external connectors are observed.

By contrast, according to the present invention, the memories of a SIP are tested by having the CPU of the SIP run testing programs that are stored in the nonvolatile memory of the SIP. This feature is neither taught nor hinted nor suggested by Malladi et al. '825. Even in the prior art of Malladi et al. '825, in which electrical signals used to test memories **13** and **15** are directed "through the microprocessor to the associated component(s) **13, 15**" (column 2 lines 36-37), these signals are determined by the external testing device as the external testing device executes its own testing program.

It follows that independent claims 18 and 23 and 26 are allowable over Malladi et al. '825. Steps (d) and (e) of claim 18 are the steps of storing in the nonvolatile memory a program for testing the nonvolatile memory and then testing the nonvolatile memory by having the CPU execute that testing program. Element (a) of claim 23 is a nonvolatile memory in which is stored a testing program for testing the nonvolatile memory. The last limitation of claim 23 is that a program for testing the volatile memory also is stored in the nonvolatile memory.

Claim 26 has been amended to render this claim allowable over Malladi et al. '825. Specifically, the step of fabricating a CPU on a third chip that is physically independent of the first two chips has been added to claim 26 as step (c), the former step (c) has been amended to state that all three components (the nonvolatile memory, the volatile memory and the CPU) are operationally connected to each other in a common package, and the former step (d) has been amended to state that the volatile memory is tested by using the CPU to execute a first testing program.

Correspondingly, steps (c) through (g) of claims 26 and 27 have been relabeled as steps (d) through (h).

Support for fabricating a CPU on a third chip that is physically independent of the other two chips is inherent in the description of the prior art of assembling SIPs on page 1 lines 13-23 of the specification:

> The advent of integrated circuits made it possible to fabricate an entire electronic circuit in a single package. Traditionally, such chips were packaged in separate packages, which then were connected together, for example after being mounted together on printed circuit boards, to form complete systems. More recently, in order to reduce the size of electronic systems further, some manufacturers have begun to package several chips, related to several technologies, in the same package. For example, a processor for controlling a cellular telephone could include a central processing unit (CPU), a nonvolatile memory such as a flash memory and a volatile memory such as a SDRAM, each fabricated on its own chip, and all packaged in the same package. Such a system is called a "System-in-Package" (SIP), a "MultiChip Package" (MCP) or a "MultiChip Module" (MCM). (emphasis added)

If the chips were packaged together in separate packages before being connected together, then the chips were inherently physically independent of each other. In a SIP, these initially physically independent chips are operationally connected and packaged together in a common package. The present invention adds to this prior art assembly process an innovative method of testing the chips that are thus assembled.

Support for the nonvolatile memory, the volatile memory and the CPU being operationally connected to each other in a common package is found in the specification in the Figure, that shows flash memory **14**, SDRAM **16** and CPU **12** operationally connected to each other in common package **18**. Support for testing the volatile memory by using the CPU to execute the first testing program is found in the specification on page 8 lines 10-11:

> ...CPU chip **12** loads program **A** from flash memory chip **14** into SDRAM chip **16**, executes program **A** in SDRAM chip **16** to test flash memory chip **14**,...

Other Amendments to the Claims

The claims have been amended generally for stylistic consistency. Specifically, everywhere that the definite article "the" is used with a claim element first introduced in the body of an independent claim or in a corresponding dependent claim rather than in the preamble of the independent claim, that definite article has been replaced with the definite article "said".

Other New Claims

Claim 3 adds to claim 1 the limitation that the CPU tests the memory by running a testing program that is loaded into one of the memories. In the case of a volatile memory, this is in contrast to Chesley '142 who tests his RAMs by executing a testing program in one of his ROMs. Therefore, new claim 30 has been added. New claim 30 is claim 3 of the response filed May 8, 2006, rewritten in independent form, and with the additional limitation that the memory is a volatile memory. Support for the memory being a volatile memory is found in the specification in SDRAM **16** of the Figure.

New claims 31 and 32 are claims 1 and 7 as now amended, without the step of testing the CPU, this step not being needed to distinguish the present invention from the cited prior art.

In view of the above amendments and remarks it is respectfully submitted that independent claims 1, 7, 18, 23, 26 and 29-32, and hence dependent claims 2, 3, 5, 6, 8, 10-17, 19-22, 27 and 28 are in condition for allowance. Prompt notice of allowance is respectfully and earnestly solicited.

Respectfully submitted,

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